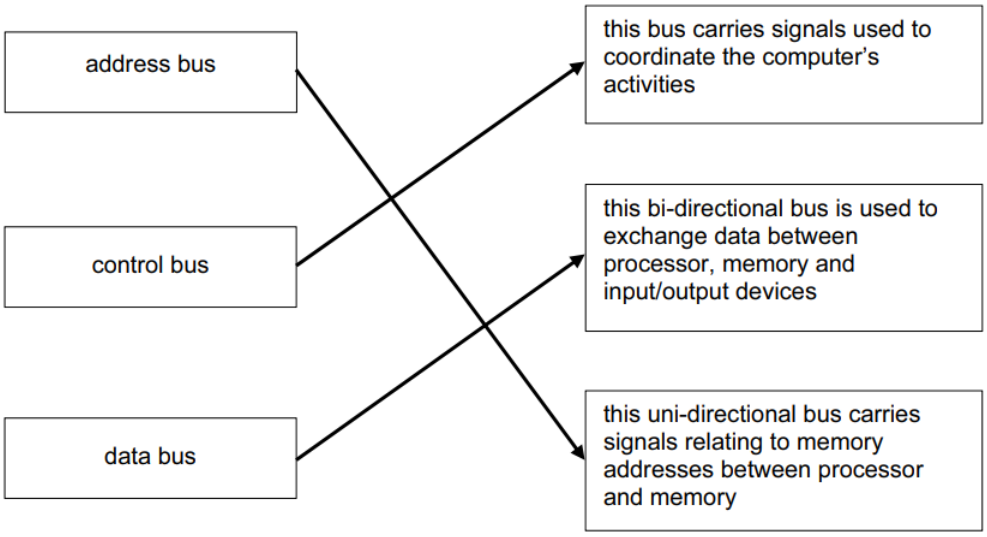
3. Hardware

3.1 Computer architecture

Marking Scheme

Q1)

(a)



2/3 matches – 2 marks
1 match – 1 mark

[2]

(b)

description of stage	sequence number
the instruction is then copied from the memory location contained in the MAR (memory address register) and is placed in the MDR (memory data register)	**3**
the instruction is finally decoded and is then executed	**7**
the PC (program counter) contains the address of the next instruction to be fetched	*(1)*
the entire instruction is then copied from the MDR (memory data register) and placed in the CIR (current instruction register)	**4**
the address contained in the PC (program counter) is copied to the MAR (memory address register) via the address bus	**2**
the address part of the instruction is placed in the MAR (memory address register)	**6**
the value in the PC (program counter) is then incremented so that it points to the next instruction to be fetched	**5***

The incrementation of the program counter can appear at any stage after 2. All other stages must be in the correct given order. [6]

Q2)

(b) Registers

Any **two** from:
- PC (Program Counter)
- MAR (Memory Address Register)
- MDR (Memory Data Register)
- CIR or IR ((Current) Instruction Register)
- ACC (Accumulator)

Buses

Any **two** from:
- control
- data
- address

[4]

Q3)

(a) (i)

MAR	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**1**

MDR	**0**	**1**	**0**	**1**	**0**	**0**	**0**	**1**

[2]

(ii)

MAR	**1**	**0**	**0**	**0**	**1**	**1**	**1**	**0**

MDR	**0**	**1**	**1**	**1**	**1**	**0**	**0**	**1**

[2]

(iii)

Address	Contents
1000 0000	0110 1110
1000 0001	0101 0001
1000 0010	1000 1101
1000 0011	1000 1100
1000 1100	
1000 1101	
1000 1110	**0111 1001**
1000 1111	

[1]

(b) – CIR (Current Instruction Register)
– PC (Program Counter)
– Acc (Accumulator) [3]

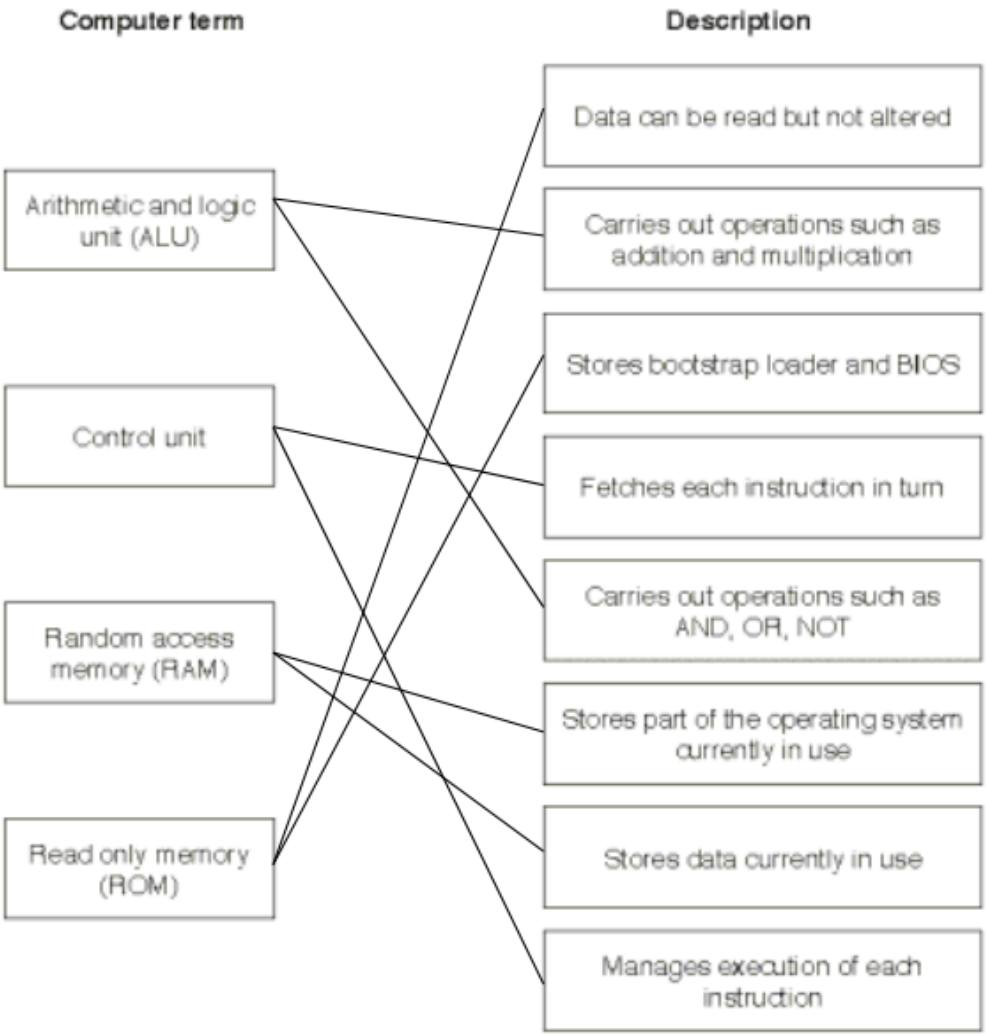
(c) – Controls operation of memory, processor and input/output
– Instructions are interpreted
– Sends signals to other components telling them "what to do" [3]

Q4)

In any order:
– Fetch
– Decode
– Execute [3]

Q5)

1 mark for **both** correct lines from each computer term.



[4]

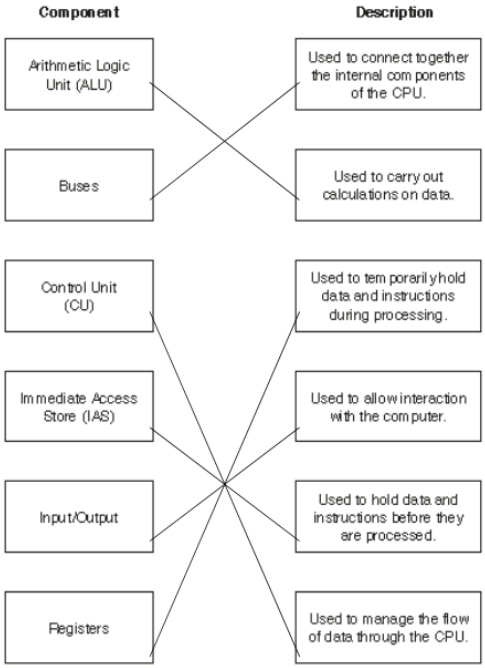
Q6)

Question	Answer	Marks
	1 mark for correct bus name and up to 2 further marks for appropriate purpose. **Address (bus)** **Two** from: ∞ Carries / transports an address / location … ∞ … of the next item to be fetched ∞ Data travels one way (unidirectional) **Data (bus)** **Two** from: ∞ Carries / transports data / example of data ... ∞ … that is currently being processed // that will be / has been processed ∞ Data can travel in both directions (bidirectional) **Control (bus)** **Two** from: ∞ Carries / transports signals ∞ Control / directs the actions of the CPU / processor ∞ Can be either Unidirectional or Bidirectional	**6**

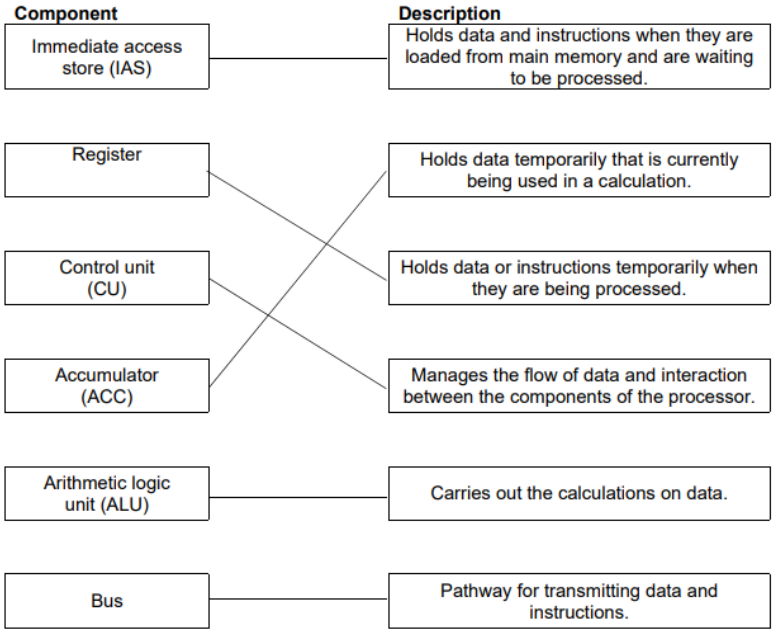
Q7)

Question	Answer	Marks
	∞ address (bus) ∞ control (bus) ∞ data (bus)	**3**

Q8)

Question	Answer	Marks
	1 mark for each correct line up to a total of 5 marks 	5

Q9)

Question	Answer	Marks
	1 mark for each correct line, up to a maximum of 5 marks: 	5

Q10)

Question	Answer	Marks
	1 mark for each correct missing word, in the given order: – fetches – immediate access store // IAS – program counter // PC – memory address register // MAR – memory data register // MDR – executed – arithmetic logic unit // ALU – accumulator // ACC	8

Q11)

Question	Answer	Marks
	Any **six** from: – Program counter (PC) holds address / location of the instruction – The address held in PC is sent to MAR – Address is sent using address bus – PC is incremented – The instruction is sent from address in memory to MDR – Instruction is transferred using the data bus – Instruction sent to CIR	6

Q12)

Question	Answer	Marks
(a)	∝ Holds address of next/current instruction … ∞ … to be fetched/processed/executed	2
(b)	∝ Stores data/instruction **that is in use …** ∞ … from address in MAR	2

Q13)

Question	Answer	Marks
	1 mark for each correct term, in the correct place: – Data/instructions – Instructions/data (must be the alternative to MP1) – Fetched – RAM – Decoded – Executed	6

Q14)

<table>
<tr><th>Question</th><th>Answer</th><th>Marks</th></tr>
<tr><td>(a)</td><td>1 mark for each correct row:

<table>
<tr><th>Statement</th><th>True (✓)</th><th>False (✓)</th></tr>
<tr><td>A MAC address is unique to a computer on a network</td><td>✓</td><td></td></tr>
<tr><td>Once an IP address has been set it cannot be changed</td><td></td><td>✓</td></tr>
<tr><td>A MAC address is made up of the computer's serial number and the IP address</td><td></td><td>✓</td></tr>
<tr><td>If a computer does not have an IP address it cannot communicate with another device using the Internet</td><td>✓</td><td></td></tr>
</table></td><td>4</td></tr>
<tr><td>(b)(i)</td><td>Two from:

– Programs / instructions are stored in memory
– Data is stored in memory
– Instructions are fetched and executed one after another</td><td>2</td></tr>
<tr><td>(b)(ii)</td><td>– Carries out calculations
– Carries out logical operations
– Holds temporary / interim values during calculations
– … in a register called the accumulator (ACC)</td><td>4</td></tr>
</table>

<table>
<tr><th>Question</th><th>Answer</th><th>Marks</th></tr>
<tr><td>(c)(i)</td><td>– Interrupt</td><td>1</td></tr>
<tr><td>(c)(ii)</td><td>Two from:

– Provides an interface
– Loads / opens / installs / closes software
– Manages the hardware // manages peripherals // spooling
– Manages the transfer of programs into and out of memory
– Divides processing time // processor management
– Manages file handling
– Manages error handling // interrupt handling
– Manages security software
– Manages utility software
– Manages user accounts
– Multitasking
– Multiprogramming // time slicing
– Batch processing</td><td>2</td></tr>
</table>

Q15)

Question	Answer	Marks
	Six from: ∞ PC holds address of the instruction ∞ The address held in PC is sent to MAR … ∞ … using address bus ∞ MAR goes to location in memory where instruction is stored ∞ Instruction sent to MDR … ∞ … using data bus ∞ Instruction sent to CIR ∞ Control unit sends signals to manage the process … ∞ … using the control bus	**6**

Q16)

Question	Answer	Marks
	Four from: ∞ Arithmetic and logic unit (ALU) ∞ Memory address register (MAR) ∞ Memory data register (MDR) // Memory buffer register (MBR) ∞ Accumulator (ACC) ∞ Immediate Access Store (IAS) ∞ Main memory // RAM ∞ Program counter (PC) ∞ Current instruction register (CIR) ∞ Address bus ∞ Data bus ∞ Control bus ∞ Input device ∞ Output device ∞ Secondary storage device	**4**

Q17)

Question	Answer	Marks
(a)(i)	**Three** from: ∞ RAM ∞ Primary memory ∞ Volatile memory ∞ Holds currently in use data/instructions ∞ Directly accessed by the CPU	**3**
'(a)(ii)	**Two** from: ∞ Arithmetic and logic unit (ALU) ∞ Memory address register (MAR) ∞ Memory data register (MDR) // Memory buffer register (MBR) ∞ Accumulator (ACC) ∞ Immediate Access Store (IAS) ∞ Control Unit (CU) ∞ Program counter (PC) ∞ Current instruction register (CIR) ∞ Address bus ∞ Data bus ∞ Control bus ∞ Input device ∞ Output device ∞ Secondary storage device	**2**

Q18)

Question	Answer	Marks
	<table><tr><th>Component</th><th>CPU component (✓)</th><th>Not a CPU component (✓)</th></tr><tr><td>Arithmetic logic unit (ALU)</td><td>✓</td><td></td></tr><tr><td>Hard disk drive (HDD)</td><td></td><td>✓</td></tr><tr><td>Memory address register (MAR)</td><td>✓</td><td></td></tr><tr><td>Random access memory (RAM)</td><td></td><td>✓</td></tr><tr><td>Solid state drive (SSD)</td><td></td><td>✓</td></tr><tr><td>Control unit (CU)</td><td>✓</td><td></td></tr></table> **One** mark per each correct row	6

Q19)

Question	Answer	Marks
(a)	Any **three** from: – MAR – MDR // MBR – PC // IAR // NIR // SCR – ACC – CIR // IR – IAS	3
(b)(i)	– Fetch – Execute	2
(b)(ii)	– Control unit	1

Q20)

Question	Answer	Marks
(a)(i)	– Uses multiple wires – Sends multiple bits of data at a time	2
(a)(ii)	– Faster transmission speed	1
(b)(i)	– Control (bus)	1
(b)(ii)	– Accumulator (ACC)	1
(b)(iii)	<table><tr><th>Statement</th><th>True (✓)</th><th>False (✓)</th></tr><tr><td>Data and instructions are stored in the same memory unit</td><td>✓</td><td></td></tr><tr><td>The control unit manages operations within the CPU</td><td>✓</td><td></td></tr><tr><td>Data and instructions can be fetched into the CPU at the same time</td><td></td><td>✓</td></tr><tr><td>The control unit is responsible for decoding an instruction</td><td>✓</td><td></td></tr></table>	4

Q21)

Question	Answer	Marks
(a)	– Control unit // CU	1
(b)	– Arithmetic logic unit // ALU	1
(c)	– Program counter // memory address register // PC // MAR	1
(d)	– Memory data register // current instruction register // MDR // CIR	1
(e)	– Memory data register // MDR	1

Q22)

<table>
<tr><th>Question</th><th>Answer</th><th>Marks</th></tr>
<tr><td>(a)</td><td>One mark per each correct row
<table>
<tr><th>Statement</th><th>ALU (✓)</th><th>CU (✓)</th><th>RAM (✓)</th></tr>
<tr><td>Stores data and instructions before they enter the central processing unit (CPU)</td><td></td><td></td><td>✓</td></tr>
<tr><td>Contains a register called the accumulator</td><td>✓</td><td></td><td></td></tr>
<tr><td>Manages the transmission of data and instructions to the correct components</td><td></td><td>✓</td><td></td></tr>
<tr><td>Contained within the CPU</td><td>✓</td><td>✓</td><td></td></tr>
<tr><td>Uses the data bus to send data into or out of the CPU</td><td>(✓)</td><td></td><td>✓</td></tr>
<tr><td>Carries out calculations on data</td><td>✓</td><td></td><td></td></tr>
</table></td><td>6</td></tr>
<tr><td>(b)</td><td>Any two from:
– MAR
– MDR // MBR
– PC
– CIR // IR</td><td>2</td></tr>
</table>

Q23)

<table>
<tr><th>Question</th><th>Answer</th><th>Marks</th></tr>
<tr><td>(a)</td><td>One mark per each correct row.

<table>
<tr><th>Statement</th><th>MAR (✓)</th><th>MDR (✓)</th><th>PC (✓)</th></tr>
<tr><td>it is a register in the CPU</td><td>✓</td><td>✓</td><td>✓</td></tr>
<tr><td>it holds the address of the next instruction to be processed</td><td>(✓)</td><td></td><td>✓</td></tr>
<tr><td>it holds the address of the data that is about to be fetched from memory</td><td>✓</td><td></td><td>(✓)</td></tr>
<tr><td>it holds the data that has been fetched from memory</td><td></td><td>✓</td><td></td></tr>
<tr><td>it receives signals from the control unit</td><td>✓</td><td>✓</td><td>✓</td></tr>
<tr><td>it uses the address bus to send an address to another component</td><td>✓</td><td></td><td>✓</td></tr>
</table></td><td>6</td></tr>
<tr><td>(b)</td><td>– Arithmetic Logic Unit // ALU</td><td>1</td></tr>
</table>

Q24)

Question	Answer	Marks
	One mark per correct term or description.	6

Component name	Description
Memory Address Register (MAR)	(A register that) holds the address of the data/instruction that needs to be fetched/processed // holds the address of where the data needs to be stored.
Program Counter (PC)	(A register that) holds the address of the **next** / **current instruction** to be processed.
accumulator // ACC	This is a register that is built into the arithmetic logic unit. It temporary holds the result of a calculation.
memory data register // MDR	This is a register that holds data or an instruction that has been fetched from memory.
Control Unit (CU)	Sends control signals to control the flow of data through the CPU // manages the execution of instructions in the CPU
address bus	This carries addresses around the CPU.

Q25)

Question	Answer	Marks
(a)	**One** mark for each correctly circled storage device: • Compact disk (CD) • Solid-state drive (SSD) • Hard disk drive (HDD)	3
(b)	• C	1

Q26)

Question	Answer	Marks
(a)	Any **one** from: • To perform a fetch-decode-execute cycle • To **process** / **execute** an instruction	1
(b)	**Two** from: • It may increase the performance • … because more instructions can be processed **simultaneously**	2
(c)(i)	**Two** from: • To store / holds **data** / **address** / **instruction** • … temporarily	2

Question	Answer	Marks
(c)(ii)	**One** mark for correct name of bus. **Two** marks for matching description. Address bus Transmit / carries addresses … … between **components** in the CPU Data bus Transmit / carries data … … between **components** in the CPU Control bus Transmits control signals … … from the **control unit** to other **components** in the CPU	3

Q27)

(c)	– Control unit	1
(d)	Any **two** from: – (The CPU completes) 2.4 billion – … cycles/clock pulses **per second**	2
(e)(i)	Any **two** from: – Stores data … – … that has been fetched/to be written to memory	2
(e)(ii)	Any **three** from: – Memory address register // MAR – Program counter // PC – Current instruction register // CIR – Accumulator // ACC	3

Q28)

Question	Answer	Marks
(a)(i)	– The maximum number of FDE cycles/instructions a CPU can perform/process/execute in a second	1
(a)(ii)	– Increases/improves the performance // Tasks can be performed quicker/faster – … because more FDE cycles/instructions can be processed in a second	2
(b)	– **Stores** addresses … – … of next instruction/data to be fetched // where data is to be written to	2
(c)	– Instruction set	1

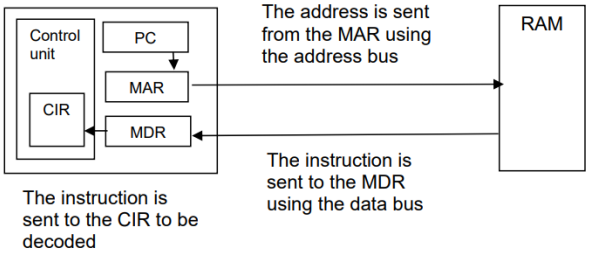
Q29)

Question	Answer	Marks
(a)	Any **two** from: – Performs a single/limited/dedicated function/task – It has a microprocessor – It has **dedicated** hardware – Uses firmware – It is normally built into a larger device/system – User normally cannot reprogram – It does not require much power – It is cheap **to manufacture** – Works automatically // works without human intervention – It is small (in size) – It is a real-time system	2
(b)	**One** mark for each correct system: – security light system – freezer – vending machine	3

Q30)

Question	Answer	Marks
(a)	– Accumulator (ACC) – Control unit (CU) – Program counter (PC)	3
(b)	Any **two** from: – It is a type of storage – …that stores **frequently used** data/instructions – To speed up **access** – … as it is faster to access than RAM – It has different levels e.g. L1 – L3	2
(c)	– Clock	1
(d)	– Arithmetic logic unit // ALU	1

Q31)

Question	Answer	Marks
(d)	Any **four** from: The diagram shows: • The registers MAR, MDR and PC • **Address** sent from PC to MAR • …using address bus (award anywhere for correct use of address bus) • …PC is incremented • **Address** sent from MAR to RAM • **Data/instruction** sent from RAM to MDR • …using data bus (award anywhere for correct use of data bus) • **Data/instruction** sent from MDR to CIR/CU • Control unit sending control sig[illegible] any part of the process • … using control bus (award anywhere for correct use of control bus) Example: PC sends address to MAR then increments 	4

Q32)

Question	Answer	Marks
(a)	**One** mark for each correct term in the correct place: • address • memory address register // MAR • random access memory // RAM • memory data register // MDR • data • current instruction register // CIR • control unit // CU	**7**
(b)	A **list** of (machine code) **commands** that can be processed by the CPU	**1**

Q33)

Question	Answer	Marks
(a)	To process instructions/data To **run** the fetch–decode–execute **cycle**	**2**
(b)(i)	Any **one** from: • To **temporarily** store data/instruction/address • To allow **immediate access** to data during the FDE cycle	**1**
(b)(ii)	Any **three** from: • Memory address register // MAR • Memory data register // MDR • Accumulator // ACC • Program counter // PC • Current instruction register // CIR	**3**
(c)	Any **three** from: • To execute **instructions** • To perform calculations // by example • To perform logical operations // by example • To store interim **results** of calculations • Stores/reads/writes data to/from the accumulator	**3**
(d)	Any **Four** from: • It could have more cores • … increasing the **number of FDE cycles/instructions** it can perform **at the same time** • It could have a higher clock speed • … increasing the **number of FDE cycles/instructions per second** it can perform • It could have a greater cache size • … meaning more **frequently used** data can be accessed faster	**4**

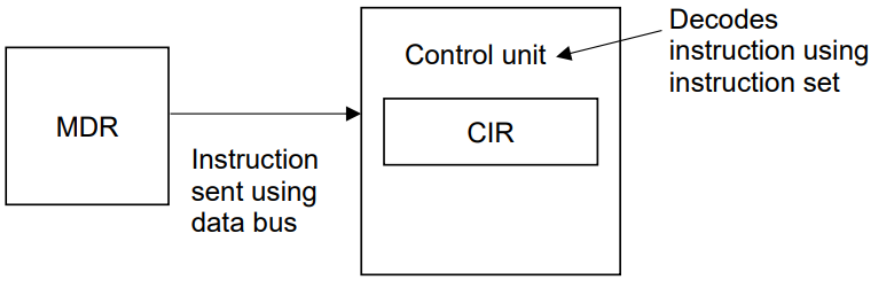
Q34)

Question	Answer	Marks
(a)	Any **two** from: • Program counter // PC • Memory address register // MAR • Memory data register // MDR • Current instruction register // CIR	**2**
(b)	Any **three** from: • **CIR/CU** receives the instruction from the **MDR** // Instruction sent from **MDR** to **CIR/CU** • … using the data bus • Instruction is **separated** into opcode and operand • Control unit decodes the **instruction** • … using an instruction set	**3**
(c)	Any **one** from: • Accumulator • Memory address register // MAR • Memory data register // MDR	**1**
(d)	• data • address • control	**3**
(e)	• It can now execute **more** instructions/FDE **per second** • … this will increase the performance of the CPU	**2**

Q35)

Question	Answer	Marks
	One mark for each correct term or definition in the correct place: **Components** • Control unit // CU • Memory address register // MAR • Data bus • Current instruction register // CIR **Descriptions** • (Program counter) Stores the address of the next instruction to be fetched • (Accumulator) Stores the interim **result** for a calculation	**6**

Q36)

Question	Answer	Marks
(a)	Any **two** from: • Program counter // PC • Memory address register // MAR • Current instruction register // CIR	**2**
(b)	**One** mark for each correct part of the diagram. The diagram shows: • Data/Instruction sent from the MDR to the CIR/CU • … using the data bus • … the CIR that is built into the CU • Data/instruction separated into operand and op code • Control unit/CU decodes instruction • … using an instruction set For example: 	**4**